In the claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) An integrated circuit device, comprising:

a semiconductor substrate;

a first memory array on the substrate comprising charge storage, nonvolatile memory cells,-configured to store data for a first pattern of data usage in response to a first operation algorithm, with the first memory array including first memory cells having a first cell structure;

a second memory array on the substrate comprising charge storage, nonvolatile memory cells, configured to store data for a second pattern of data usage and facilitate bit-by-bit erasure of data in said second memory array in response to a second operation algorithm, with the second memory array including second memory cells having a second cell structure that is substantially the same as the first cell structure; and

controller circuitry coupled to the first and second memory arrays, including logic to read, program and erase data in the first memory array and in the second memory array according to the first and second operation algorithms.

2. (original) The integrated circuit device of claim 1, wherein the charge storage, nonvolatile memory cells in the first memory array respectively comprise a first channel terminal, a channel, and a second channel terminal in the substrate, a first dielectric layer, a charge trapping structure and a second dielectric layer overlying the channel, and a gate terminal.

3. (original) The integrated circuit device of claim 1, wherein the charge storage, nonvolatile memory cells in the first memory array and in the second memory array respectively comprise a first channel terminal, a channel, and a second channel terminal in the substrate, a first dielectric layer, a charge trapping structure and a second dielectric layer overlying the channel, and a gate terminal.

4. (original) The integrated circuit device of claim 1, wherein the charge storage, nonvolatile memory cells in the first memory array and in the second memory array respectively comprise a first channel terminal, a channel, and a second channel terminal in the substrate, a first dielectric

layer, a charge trapping structure and a second dielectric layer overlying the channel, and a gate terminal, and wherein the charge trapping structure comprises at least one of silicon nitride, Al_2O_3, HfO_x, ZrO_x, or other metal oxide.

5. (canceled)

6. (original) The integrated circuit device of claim 1, wherein the first operation algorithm includes programming by hole injection.

7. (original) The integrated circuit device of claim 1, wherein the first operation algorithm includes programming by band-to-band tunneling induced hole injection.

8. (original) The integrated circuit device of claim 1, wherein the first operation algorithm includes erasing by E-field assisted electron injection.

9. (original) The integrated circuit device of claim 1, wherein the first operation algorithm includes programming by hole injection, and erasing by E-field assisted electron injection.

10. (original) The integrated circuit device of claim 1, wherein the second operation algorithm includes programming by electron injection.

11. (original) The integrated circuit device of claim 1, wherein the second operation algorithm includes programming by channel electron injection.

12. (original) The integrated circuit device of claim 1, wherein the second operation algorithm includes erasing by hole injection.

13. (original) The integrated circuit device of claim 1, wherein the second operation algorithm includes erasing by band-to-band tunneling induced hole injection.

14. (original) The integrated circuit device of claim 1, wherein the second operation algorithm includes programming by electron injection, and erasing by hole injection.

15. (original) The integrated circuit device of claim 1, wherein the first operation algorithm includes programming by hole injection, and erasing by E-field assisted electron injection, and the second operation algorithm includes programming by electron injection, and erasing by hole injection.

16. (original) The integrated circuit device of claim 1, wherein the charge storage, nonvolatile memory cells include flash memory cells having substantially the same structure in the first memory array and in the second memory array, and the first operation algorithm includes programming by hole injection, and erasing by E-field assisted electron injection, and the second operation algorithm includes programming by electron injection, and erasing by hole injection.

17. (original) The integrated circuit device of claim 1, wherein the charge storage, nonvolatile memory cells in the first memory array and in the second memory array include flash memory cells having substantially the same structure with nitride charge trapping structures.

18. (original) The integrated circuit device of claim 1, wherein the charge storage, nonvolatile memory cells in the first memory array and in the second memory array include flash memory cells having substantially the same structure with nitride charge trapping structures, and the first operation algorithm includes programming by hole injection, and erasing by E-field assisted electron injection, and the second operation algorithm includes programming by electron injection, and erasing by hole injection.

19. (original) The integrated circuit device of claim 1, wherein the charge storage, nonvolatile memory cells in the first memory array and in the second memory array include flash memory cells that are adapted to store two bits per memory cell.

20. (original) The integrated circuit device of claim 1, wherein the charge storage, nonvolatile memory cells in the first memory array and in the second memory array include flash memory cells that are adapted to store two bits per memory cell, and further the first operation algorithm includes programming by hole injection, and erasing by E-field assisted electron injection, and

the second operation algorithm includes programming by electron injection, and erasing by hole injection.

21. (original) The integrated circuit device of claim 1, wherein the controller circuitry is on the semiconductor substrate.

22. (original) The integrated circuit device of claim 1, including an SRAM array and a user programmable processor on the semiconductor substrate coupled with the first and second memory arrays.

23. (Currently Amended) A method for manufacturing an integrated circuit device, comprising:

providing a semiconductor substrate;

forming a first memory array on the substrate comprising charge storage, nonvolatile memory cells, configured to store data according to a first pattern of data usage in response to a first operation algorithm, with the first memory array including first memory cells having a first cell structure;

forming a second memory array on the substrate comprising charge storage, nonvolatile memory cells, configured to store data according to a second pattern of data usage and facilitate bit-by-bit erasure of data in said second memory array in response to a second operation algorithm, with the second memory array including second memory cells having a second cell structure that is substantially the same as the first cell structure; and

providing controller circuitry coupled to the first and second memory arrays, to read, program and erase data in the first memory array and in the second memory array according to the first and second operation algorithms.

24. (original) The method for manufacturing of claim 23, wherein forming the first memory array comprises forming a plurality of memory cells by making a first channel terminal, a channel, and a second channel terminal in the substrate, and building charge storage structure including a first dielectric layer, a charge trapping structure and a second dielectric layer overlying the channel, and a gate terminal overlying the second dielectric layer.

25. (original) The method for manufacturing of claim 23, wherein forming the first memory array and forming a second memory array comprises using a set of process steps which results in simultaneously forming a first plurality of bitlines for the first memory array and a second plurality of bitlines for the second memory array, and simultaneously forming a first plurality of wordlines in the first memory array and a second plurality of wordlines and a second memory array.

26. (original) The method for manufacturing of claim 23, wherein forming the first memory array and forming a second memory array comprises using a set of process steps which results in simultaneously forming a first plurality of bitlines for the first memory array and a second plurality of bitlines for the second memory array, simultaneously forming charge storage structures for memory cells in the first memory array and in the second memory array, and simultaneously forming a first plurality of wordlines in the first memory array and a second plurality of wordlines and a second memory array.

27. (original) The method for manufacturing of claim 23, wherein the charge storage, nonvolatile memory cells in the first memory array and in the second memory array respectively comprise a first channel terminal, a channel, and a second channel terminal in the substrate, a first dielectric layer, a charge trapping structure and a second dielectric layer overlying the channel, and a gate terminal, and wherein the charge trapping structure comprises at least one of silicon nitride, Al_2O_3, HfO_x, ZrO_x, or other metal oxide.

28. (canceled)

29. (previously presented) The method for manufacturing of claim 23, wherein the first operation algorithm includes programming by hole injection.

30. (previously presented) The method for manufacturing of claim 23, wherein the first operation algorithm includes programming by band-to-band tunneling induced hole injection.

31. (previously presented) The method for manufacturing of claim 23, wherein the first operation algorithm includes erasing by E-field assisted electron injection.

32. (previously presented) The method for manufacturing of claim 23, wherein the first operation algorithm includes programming by hole injection, and erasing by E-field assisted electron injection.

33. (previously presented) The method for manufacturing of claim 23, wherein the second operation algorithm includes programming by electron injection.

34. (previously presented) The method for manufacturing of claim 23, wherein the second operation algorithm includes programming by channel hot electron injection.

35. (previously presented) The method for manufacturing of claim 23, wherein the second operation algorithm includes erasing by hole injection.

36. (previously presented) The method for manufacturing of claim 23, wherein the second operation algorithm includes erasing by band-to-band tunneling induced hole injection.

37. (previously presented) The method for manufacturing of claim 23, wherein the second operation algorithm includes programming by electron injection, and erasing by hole injection.

38. (previously presented) The method for manufacturing of claim 23, wherein the first operation algorithm includes programming by hole injection, and erasing by E-field assisted electron injection, and the second operation algorithm includes programming by electron injection, and erasing by hole injection.

39. (previously presented) The method for manufacturing of claim 23, wherein the charge storage, nonvolatile memory cells in the first memory array and in the second memory array include flash memory cells with nitride charge trapping structures, and the first operation algorithm includes programming by hole injection, and erasing by E-field assisted electron injection, and the second operation algorithm includes programming by electron injection, and erasing by hole injection.

40. (previously presented) The method for manufacturing of claim 23, wherein the charge storage, nonvolatile memory cells in the first memory array and in the second memory array include flash memory cells with nitride charge trapping structures which are substantially the same.

41. (previously presented) The method for manufacturing of claim 23, wherein the charge storage, nonvolatile memory cells in the first memory array and in the second memory array include flash memory cells with nitride charge trapping structures which are substantially the same, and further the first operation algorithm includes programming by hole injection, and erasing by E-field assisted electron injection, and the second operation algorithm includes programming by electron injection, and erasing by hole injection.

42. (previously presented) The method for manufacturing of claim 23, wherein the charge storage, nonvolatile memory cells in the first memory array and in the second memory array include flash memory cells that are adapted to store two bits per memory cell.

43. (previously presented) The method for manufacturing of claim 23, wherein the charge storage, nonvolatile memory cells in the first memory array and in the second memory array include flash memory cells that are adapted to store two bits per memory cell, and further the first operation algorithm includes programming by hole injection, and erasing by E-field assisted electron injection, and the second operation algorithm includes programming by electron injection, and erasing by hole injection.

44. (previously presented) The method for manufacturing of claim 23, including forming an SRAM array and a user programmable processor on the semiconductor substrate coupled with the first and second memory arrays.

45. (Currently Amended) A method for storing data and code on a single integrated circuit, comprising:

addressing a first memory array comprising nonvolatile memory cells on the integrated circuit, to read, program and erase first data;

addressing a second memory array comprising nonvolatile memory cells on the

integrated circuit, to read, program and erase second data;

reading, programming and erasing first data in the first memory array according to a first operation algorithm adapted for a first pattern of data usage, with the first memory array including first memory cells having a first cell structure; and

reading, programming and erasing **[[code]]** second data in the second memory array according to a second operation algorithm adapted for a second pattern of data usage, the second memory array including second memory cells having a second cell structure that is substantially the same as the first cell structure, wherein the second operation algorithm is not the same as the first operation algorithm, with erasing said second data occurring bit-by-bit.

46. (previously presented) The method of claim 45, wherein the nonvolatile memory cells in the first memory array and the second memory array comprise charge storage memory cells.

47. (previously presented) The method of claim 45, wherein the nonvolatile memory cells in the first memory array and the second memory array comprise charge trapping memory cells having charge trapping structures, and wherein the charge trapping structures comprise at least one of silicon nitride, Al_2O_3, HfO_x, ZrO_x, or other metal oxide.

48. (previously presented) The method of claim 45, wherein the nonvolatile memory cells in the first memory array are adapted for data storage by charge trapping, and the nonvolatile memory cells in the second memory array are adapted for data storage by charge trapping.

49. (canceled)

50. (previously presented) The method of claim 45, wherein the first operation algorithm includes programming by hole injection.

51. (previously presented) The method of claim 45, wherein the first operation algorithm includes programming by band-to-band tunneling induced hole injection.

52. (previously presented) The method of claim 45, wherein the first operation algorithm includes erasing by E-field assisted electron injection.

53. (previously presented) The method of claim 45, wherein the first operation algorithm includes programming by hole injection, and erasing by E-field assisted electron injection.

54. (previously presented) The method of claim 45, wherein the second operation algorithm includes programming by electron injection.

55. (previously presented) The method of claim 45, wherein the second operation algorithm includes programming by channel hot electron injection.

56. (previously presented) The method of claim 45, wherein the second operation algorithm includes erasing by hole injection.

57. (previously presented) The method of claim 45, wherein the second operation algorithm includes erasing by band-to-band tunneling induced hole injection.

58. (previously presented) The method of claim 45, wherein the second operation algorithm includes programming by electron injection, and erasing by hole injection.

59. (previously presented) The method of claim 45, wherein the first operation algorithm includes programming by hole injection, and erasing by E-field assisted electron injection, and the second operation algorithm includes programming by electron injection, and erasing by hole injection.

60. (previously presented) The method of claim 45, wherein the charge storage, nonvolatile memory cells in the first memory array and in the second memory array include flash memory cells with nitride charge trapping structures, and the first operation algorithm includes programming by hole injection, and erasing by E-field assisted electron injection, and the second operation algorithm includes programming by electron injection, and erasing by hole injection.

61. (previously presented) The method of claim 45, wherein the charge storage, nonvolatile memory cells in the first memory array and in the second memory array include flash memory cells with nitride charge trapping structures which are substantially the same.

62. (previously presented) The method of claim 45, wherein the charge storage, nonvolatile memory cells in the first memory array and in the second memory array include flash memory cells with nitride charge trapping structures which are substantially the same, and further the first operation algorithm includes programming by hole injection, and erasing by E-field assisted electron injection, and the second operation algorithm includes programming by electron injection, and erasing by hole injection.

63. (previously presented) The method of claim 45, including storing two bits per memory cell in at least one of the first and second memory arrays.

64. (previously presented) The method of claim 45, including storing two bits per memory cell in at least one of the first and second memory arrays, and further the first operation algorithm includes programming by hole injection, and erasing by E-field assisted electron injection, and the second operation algorithm includes programming by electron injection, and erasing by hole injection.

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